**Computer Organization & Architecture**

**Fall 2013 (Mid Term -1)**

**Total marks: 40 Time: 90 Mins**

**Note : Assume any missing data or typing errors.**

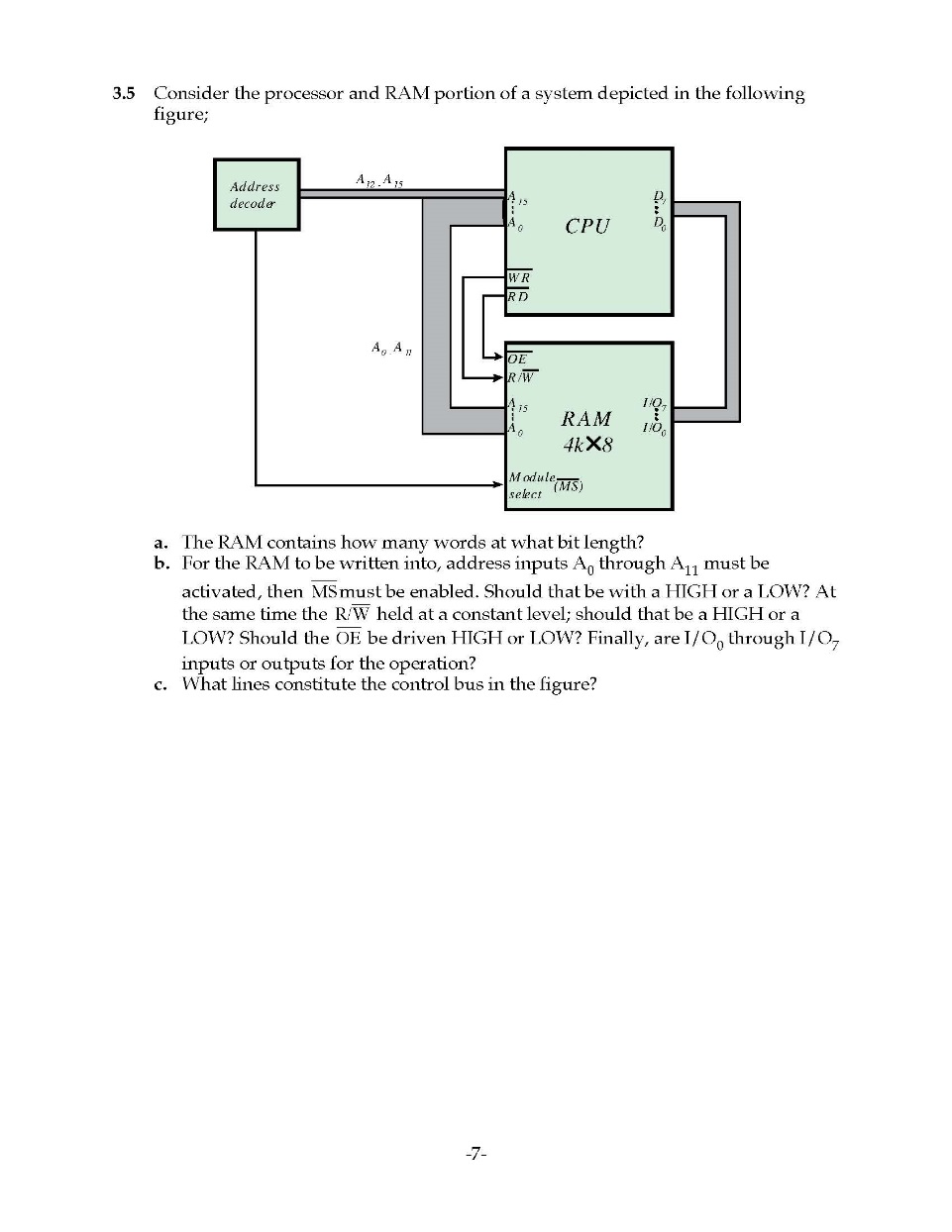
**Question#1(a). What is the benefit of using a multiple-bus architecture compared to a single-bus architecture? (5 Marks)**

**Answer#1(a). If a great number of devices are connected to the bus, performance will suffer. There are two main causes:**

**In general, the more devices attached to the bus, the greater the bus length and hence the greater the propagation delay. This delay determines the time it takes for devices to coordinate the use of the bus. When control of the bus passes from one device to another frequently, these propagation delays can noticeably affect performance.**

**The bus may become a bottleneck as the aggregate data transfer demand approaches the capacity of the bus. This problem can be countered to some extent by increasing the data rate that the bus can carry and by using wider buses (e.g., increasing the data bus from 32 to 64 bits). However, because the data rates generated by attached devices (e.g., graphics and video controllers, network interfaces) are growing rapidly, this is a race that a single bus is ultimately destined to lose.**

**Accordingly, most bus-based computer systems use multiple buses, generally laid out in a hierarchy. A typical traditional structure is shown in Figure 3.17a(S-81). There is a local bus that connects the processor to a cache memory and that may support one or more local devices. The cache memory controller connects the cache not only to this local bus, but to a system bus to which are attached all of the main memory modules. In contemporary systems, the cache is in the same chip as the processor, and so an external bus or other interconnect scheme is not needed, although there may also be an external cache. As will be discussed in Chapter 4, the use of a cache structure insulates the processor from a requirement to access main memory frequently. Hence, main memory can be moved off of the local bus onto a system bus. In this way, I/O transfers to and from the main memory across the system bus do not interfere with the processor’s activity.**

**Question#1(b). Based on figure below answer parts a & b. (3+2 Marks)**

**a. The RAM contains how many words at what bit length ?**

**b. What line constitute the control bus in the figure ?**

**Answer#1(b).**

**a. 4K Words of 8-bit each.**

**b. The line from WR to OE plus the line from RD to R/W.**

**Question#2(a). How does SDRAM differ from ordinary DRAM? (5 Marks)**

**Answer#2(a).**

**SDRAM versus ordinary DRAM**

**One of the most widely used forms of DRAM is the synchronous DRAM (SDRAM). Unlike the traditional DRAM, which is asynchronous, the SDRAM exchanges data with the processor synchronized to an external clock signal and running at the full speed of the processor/memory bus without imposing wait states.**

**In a typical DRAM, the processor presents addresses and control levels to the memory, indicating that a set of data at a particular location in memory should be either read from or written into the DRAM. After a delay, the access time, the DRAM either writes or reads the data. During the access-time delay, the DRAM performs various internal functions, such as activating the high capacitance of the row and column lines, sensing the data, and routing the data out through the output buffers. The processor must simply wait through this delay, slowing system performance.**

**With synchronous access, the DRAM moves data in and out under control of the system clock. The processor or other master issues the instruction and address information, which is latched by the DRAM. The DRAM then responds after a set number of clock cycles. Meanwhile, the master can safely do other tasks while the SDRAM is processing the request.**

**SRAM versus DRAM**

**Both volatile: Power must be continuously supplied to the memory to preserve the bit values**

**Dynamic : Simpler to build, smaller, More dense (smaller cells = more cells per unit area), Less expensive, Requires the supporting refresh circuitry, Tend to be favored for large memory requirements, Used for main memory**

**Static : Faster, Used for cache memory (both on and off chip)**

**Question#2(b). List and define two approaches to dealing with multiple interrupts. (5 Marks)**

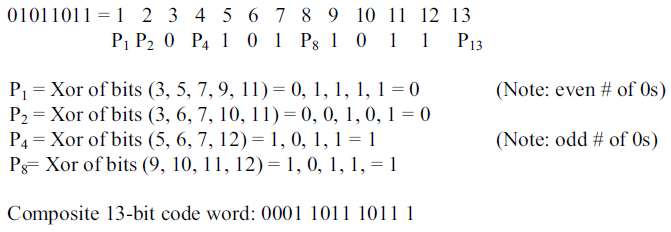
**Answer#2(b). Two approaches can be taken to dealing with multiple interrupts. The first is to disable interrupts while an interrupt is being processed. A disabled interrupt simply means that the processor can and will ignore that interrupt request signal. If an interrupt occurs during this time, it generally remains pending and will be checked by the processor after the processor has enabled interrupts. Thus, when a user program is executing and an interrupt occurs, interrupts are disabled immediately. After the interrupt handler routine completes, interrupts are enabled before resuming the user program, and the processor checks to see if additional interrupts have occurred. This approach is nice and simple, as interrupts are handled in strict sequential order (Figure 3.13a).**

**The drawback to the preceding approach is that it does not take into account relative priority or time-critical needs. For example, when input arrives from the communications line, it may need to be absorbed rapidly to make room for more input. If the first batch of input has not been processed before the second batch arrives, data may be lost.**

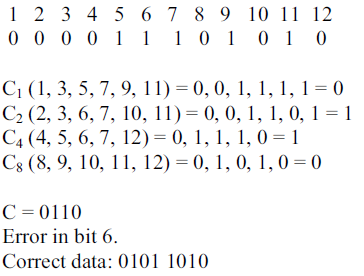
**A second approach is to define priorities for interrupts and to allow an interrupt of higher priority to cause a lower-priority interrupt handler to be itself interrupted (Figure 3.13b).**

**Question#3(a). Given the 8-bit data word 01011011, generate the 13-bit composite word for the hamming code that corrects single errors and detects double errors. Clearly label the 8-bit data, 4-bit code & 1-parity bit. (5 Marks)**

**Answer#3(a).**



**Question#3(b). A 12-bit Hamming code word containing 8 bits of data and 4 parity bits is read from the memory. What was the original 8-bit that was written into memory if the 12-bit word read out is 000011101010 ? (5 Marks)**



**Question #4 (a). How does the principle of locality relate to the use of multiple memory levels? (5 Marks)**

**Answer #4 (a). The basis for the validity of condition (d) – [Decreasing frequency of access of the memory by the processor] is a principle known as locality of reference. During the course of execution of a program, memory references by the processor, for both instructions and data, tend to cluster. Programs typically contain a number of iterative loops and subroutines. Once a loop or subroutine is entered, there are repeated references to a small set of instructions. Similarly, operations on tables and arrays involve access to a clustered set of data words. Over a long period of time, the clusters in use change, but over a short period of time, the processor is primarily working with fixed clusters of memory references.**

**Question #4 (b). Write if the following are Increasing or Decreasing As one goes down the memory hierarchy: (2 Marks)**

**a. Cost per bit**

**b. Capacity**

**c. Access time**

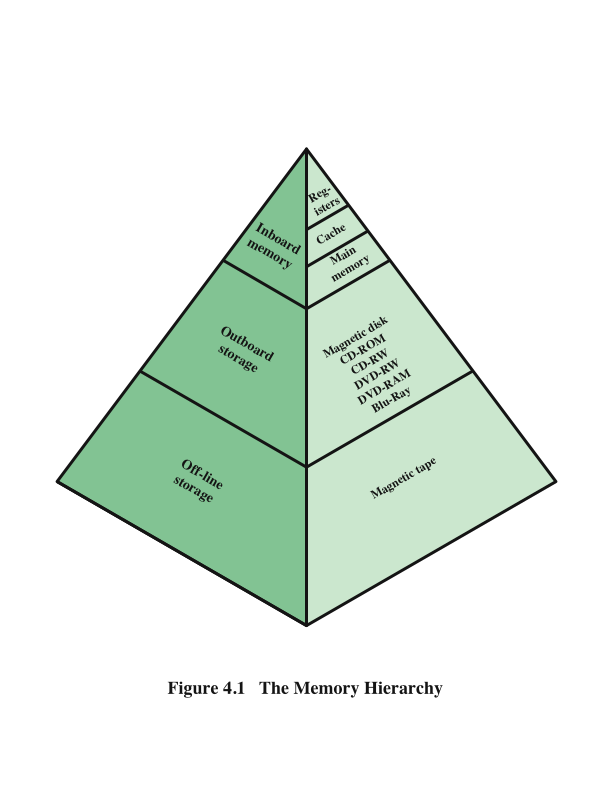
**d. Frequency of access**

**Answer #4 (b).**

1. **Decreasing cost per bit**
2. **Increasing capacity**
3. **Increasing access time**
4. **Decreasing frequency of access of the memory by the processor**

**Question #4 (c). Which of the following relationships holds false for memories: (3 Marks)**

**a. Faster access time, lesser cost per bit**

****

**b. Greater capacity, greater cost per bit**

**c. Greater capacity, faster access time**

**Answer #4 (c). (All are false.)**

1. **Faster access time (↑), greater cost per bit (↑)**
2. **Greater capacity(↑), smaller cost per bit (↓)**
3. **Greater capacity(↑), slower access time (↓)**